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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,321	12/08/2003	Toshiaki Fukushima	JP920030131US2	2430

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LENOVO (US) IP Law
Mail Stop ZHHA/B675/PO Box 12195
3039 Cornwallis Road
RTP, NC 27709-2195

EXAMINER	
VIDWAN, JASJIT S	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 07/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,321	FUKUSHIMA ET AL.	
	Examiner	Art Unit	
	Jasjit S. Vidwan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because it contains an embedded hyperlink and/or other form of browser-executable code on Page 2 under "Description of Related Art". Applicant is required to delete the embedded hyperlink and/or other form of browser-executable code. See MPEP § 608.01.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. Claims 1-14 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 reads "A program for **allowing** a processing unit to function" and therefore it's unclear what Applicant's intended metes and bounds of the claim are, since the claim appears to cover anything and everything that does not prohibit actions from occurring.

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 1-16 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 1-16 reads on a program per se for allowing a processing unit which is an absent recitation of any code or steps for causing a computer to do anything, instead just ensuring there's no code or steps which prohibit it, there does not appear to be a useful, concrete and tangible result.

Claims 1-18 is more of a functional descriptive material that fail to recite the function being executed by hardware for concrete result (i.e. setting a limit is not a real world practical application).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-18 rejected under 35 U.S.C. 102(b) as being anticipated by Pollard, II et al, U.S. Patent No: 7,050,959 **[herein after Pollard]**.

3. **As per Claim 1, 15 and 17**, Pollard teaches a program for allowing a processing unit to function as a setting device for setting a memory control device which accesses a memory module implementing a memory device therein, the program allowing the processing unit to function as:

> (a) A memory attribute information acquisition unit for acquiring memory attribute information indicating an attribute of the memory module from an attribute memory provided in the memory module **[Col. 5, Lines 26-36]**;
>
> (b) A transfer rate-setting unit **[Fig. 1, Element 110, "BIOS"]** for determining, based on the memory attribute information **[Col. 3, Lines 40-43]**, a data transfer rate setting value as a rate of an upper limit value of a data transfer rate (maximum sustainable power) relative to a maximum data transfer rate **[Col. 3, Lines 43-52 & Col. 4, Lines 32-45,** "Maximum sustainable power represents upper limit value of the data transfer"**]**, and for setting the determined data transfer rate setting value in the memory control device **[Col. 5, Lines 1-4]**, the upper limit value of the data transfer rate being at which the memory control device accesses the memory module **[Col. 3, Lines 43-52, "Maximum sustainable power"]**, and the maximum data transfer rate being at which the

memory control device is able to access the memory module **[Col. 4, Lines 46-49, "Maximum threshold bandwidth"]**.

4. **As per Claims 2**, Pollard teaches a program wherein the transfer rate setting unit determines an upper limit value of a number of memory accesses issued by the memory control device per unit time as the data transfer rate setting value based on the memory attribute information, and sets the determined upper limit value in the memory control device **[Col. 5, Lines 9-16,** "Read/write requests"**]**.

5. **As per Claim 3,** Pollard teaches a program wherein the transfer rate setting unit determines a value indicating a number of idle cycles while the memory control device is not performing memory accesses as the data transfer rate setting value based on the memory attribute information, each idle cycle being inserted between one cycle while the memory control device is performing a memory access and the other to set the determined value in the memory control device **[Col. 5, Lines 16-24]**.

6. **As per Claim 4,** Pollard teaches a program wherein the memory module generates heat by being accessed by the memory control device **[Col. 1, Lines 15-21]** and the transfer rate setting unit determines a data transfer rate setting value for maintaining a temperature of the memory module at a predetermined upper limit temperature or lower based on the memory attribute information, and sets the determined data transfer rate setting value in the memory control device **[Col. 5, Lines 4-9]**.

7. **As per Claim 5,** Pollard teaches a program wherein, as setting for maintaining the memory module at the upper limit temperature or lower, the transfer rate setting unit determines, as the data transfer rate setting value, a smaller value in a case where a heating value of the memory module is larger as compared with a value in a case where the heating value of the memory module is smaller, and sets the determined data transfer rate setting in the memory control device **[Col. 5, Lines 4-9]**.

8. **As per Claim 6,** Pollard teaches a program further comprising an upper limit temperature acquisition unit for acquiring an upper limit temperature at which the memory module is operated, wherein the transfer rate setting unit determines a data transfer rate setting value for maintaining

the temperature of the memory module at the upper limit temperature or lower based on the memory attribute information, and sets the determined data transfer rate setting value in the memory control device **[Col. 4, Lines 32-37]**.

9. **As per Claim 7**, Pollard teaches a program wherein the memory module is attached into any of a plurality of memory slots provided in an information processing apparatus **[Col. 3, Lines 58-60]**; Setting device further includes a memory attachment position information acquisition unit for acquiring memory attachment position information indicating into which of the memory slots the memory module is attached **[Col. 3, Line30-40]**; Transfer rate setting unit determines the data transfer rate setting value based on the memory attribute information and the memory attachment position information, and sets the determined data transfer rate setting value in the memory control device **[Col. 5, Lines 47-55]**.

10. **As per Claim 8**, Pollard teaches a program wherein:

The setting device is a device for setting the data transfer rates for a plurality of the memory modules **[Col. 3, Lines 58-60]** attached into an information processing apparatus **[Fig. 1, Element 110]**.

The memory attribute information acquisition unit acquires the memory attribute information of the plurality of memory modules for each thereof in association therewith **[Col. 5, Lines 26-36]**.

The transfer rate setting unit creates individual setting values as data transfer rate setting values set when the memory modules are singly attached into the information processing apparatus for each of the plurality of memory modules based on the memory attribute information of the memory modules **[Col. 3, Line 60 - Col. 4, Line 4]**, and determines a value between maximum and minimum values of the individual setting values, each of which is created so as to correspond to each of the plurality of memory modules, as a data transfer rate setting value for the plurality of memory modules **[Col. 4, Lines 33-40]**.

11. **As per Claim 9**, Pollard teaches a program wherein:

The setting device is a device for setting the data transfer rates for a plurality of the memory modules **[Col. 3, Lines 58-60]** attached into an information processing apparatus **[Fig. 1, Element 110]**.

The memory attribute information acquisition unit acquires the memory attribute information of the plurality of memory modules for each thereof in association therewith **[Col. 5, Lines 26-36]**.

The transfer rate setting unit creates individual setting values as data transfer rate setting values set when the memory modules are singly attached into the information processing apparatus for each of the plurality of memory modules based on the memory attribute information of the memory modules **[Col. 3, Line 60 - Col. 4, Line 4]**, and determines a minimum value of the individual setting values, each of which is created so as to correspond to each of the plurality of memory modules, as a data transfer rate setting value for the plurality of memory modules **[Col. 5, Lines 46-55]**.

12. **As per Claim 10**, Pollard teaches a program wherein the memory attribute information acquisition unit acquires type identification information identifying a type of any of the memory module and the memory device as the memory attribute information **[Col. 3, Lines 19-30]**, and the transfer rate setting unit determines the data transfer rate setting value in accordance with the type identification information, and sets the determined data transfer rate setting value in the memory control device **[Col. 4, Lines 33-40]**.

13. **As per Claim 11**, Pollard teaches program wherein the transfer rate setting unit determines the data transfer rate setting value in accordance with the manufacturer identification information, and sets the determined data transfer rate setting value in the memory control device **[Col. 4, Lines 54-67]**.

14. **As per Claim 12**, Pollard teaches a program wherein the memory attribute information acquisition unit acquires number-of-devices information indicating a number of the memory devices implemented in the memory module as the memory attribute information **[Col. 5, Lines 26-36]**.

15. **As per Claim 13**, Pollard teaches a program wherein the memory module includes a board implementing at least one memory device thereon **[Col. 3, Lines 58-66]**, memory attribute information acquisition unit acquires, as the memory module is a memory module of single-sided implementation, which implements the memory device on one side of the board or a memory module of double-sided implementation, which implements the memory devices on both sides of the board **[Col. 3, Lines 30-40]**. The transfer rate setting unit determines the data transfer rate setting value in accordance with the memory bank information, and sets the determined data transfer rate setting value in the memory control device **[Col. 5, Lines 1-9]**.

16. **As per Claim 14**, Pollard teaches a program wherein the transfer rate setting unit determines, as the data transfer rate setting value, a smaller value in a case where the memory bank information indicates the memory module of the double-sided implementation as compared with a value in a case where the memory bank information indicates the memory module of the single-sided implementation, and sets the determined data transfer rate setting value in the memory control device **[Col. 4, Lines 33-40]**.

17. **As per Claim 16 and 18,** Pollard teaches a system wherein the program is machine-readable program **[Col. 8, Lines 8-12]**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasjit S. Vidwan whose telephone number is (571) 272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM HUYNH can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JSV
6/26/06

KIM HUYNH
SUPERVISORY PATENT EXAMINER
6/27/06